Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (cancelled).

2. (currently amended) ~~The method of claim 1,~~ A method of fabricating PMOS and NMOS metal gate structures in a semiconductor device, the method comprising:

forming a gate dielectric in PMOS and NMOS regions above a semiconductor body;

forming a metal nitride above the gate dielectric in the NMOS region;

forming a metal boride above the gate dielectric in the PMOS region;

patterning the metal nitride to form an NMOS gate structure in the NMOS region; and

patterning the metal boride to form a PMOS gate structure in the PMOS region;

wherein forming the metal boride above the gate dielectric in the PMOS region comprises:

forming a metal nitride above the gate dielectric in the PMOS region; and

introducing boron into the metal nitride to form the metal boride in the PMOS region.

3. (original) The method of claim 2, wherein introducing boron into the metal nitride in the PMOS region comprises selectively implanting boron or boron-containing dopants into the metal nitride to form the metal boride in the PMOS region.

4. (original) The method of claim 3, wherein the boron or boron-containing dopants are implanted into the metal nitride in the PMOS region prior to forming a conductive upper material above the metal boride in the PMOS region.

5. (original) The method of claim 2, further comprising:

forming a conductive upper material above the metal nitride in the NMOS region; and

forming a conductive upper material above the metal boride in the PMOS region;

wherein the conductive upper material is formed in the PMOS region prior to introducing boron into the metal nitride in the PMOS region.

6. (original) The method of claim 5, wherein the conductive upper material is poly-silicon, and wherein introducing boron into the metal nitride in the PMOS region comprises selectively implanting boron or boron-containing dopants through the poly-silicon and into the metal nitride to form the metal boride in the PMOS region.

7. (original) The method of claim 5, wherein the conductive upper material is poly-silicon, and wherein introducing boron into the metal nitride in the PMOS region comprises:

implanting boron or boron-containing dopants into the poly-silicon in the PMOS region; and

diffusing at least some of the boron or boron-containing dopants from the poly-silicon into the metal nitride to form the metal boride in the PMOS region.

8. (original) The method of claim 2, wherein introducing boron into the metal nitride in the PMOS region comprises exposing the metal nitride to a boron-containing ambient to form the metal boride in the PMOS region.

9. (original) The method of claim 8, wherein introducing boron into the metal nitride in the PMOS region comprises annealing the metal nitride in a boron-containing ambient to form the metal boride in the PMOS region.

10. (original) The method of claim 8, wherein introducing boron into the metal nitride in the PMOS region comprises exposing the metal nitride to a plasma in the boron-containing ambient to form the metal boride in the PMOS region.

11. (original) The method of claim 2, wherein introducing boron into the metal nitride in the PMOS region comprises:

forming a boron-containing material over the metal nitride; and

diffusing boron from the boron-containing material into the metal nitride to form the metal boride in the PMOS region.

12. (original) The method of claim 2, wherein the metal nitride is one of M_XN_Y, $M_XSi_YN_Z$, $M_XAl_YN_Z$, and $M_WAl_XSi_YN_Z$, where M is one of Ti, Ta, Hf, Zr, and W.

13. (original) The method of claim 2, wherein the metal boride is one of M_XB_Y, $M_XSi_YB_Z$, $M_XAl_YB_Z$, and $M_WAl_XSi_YB_Z$ where M is one of Ti, Ta, Hf, Zr, and W.

14. (original) The method of claim 2, wherein the metal nitride is TiN and the metal boride is TiB_2.

15-17. (cancelled).

18. (currently amended) ~~The method of claim 1,~~ A method of fabricating PMOS and NMOS metal gate structures in a semiconductor device, the method comprising:

forming a gate dielectric in PMOS and NMOS regions above a semiconductor body;

forming a metal nitride above the gate dielectric in the NMOS region;

forming a metal boride above the gate dielectric in the PMOS region;

patterning the metal nitride to form an NMOS gate structure in the NMOS region; and

patterning the metal boride to form a PMOS gate structure in the PMOS region;

wherein forming metal nitride above the gate dielectric in the NMOS region comprises:

forming metal boride above the gate dielectric in the NMOS region; and

introducing nitrogen into the metal boride to form the metal nitride in the PMOS region.

19. (original) The method of claim 18, wherein introducing nitrogen into the metal boride comprises performing an ammonia anneal to form the metal nitride in the PMOS region.

20. (original) The method of claim 18, wherein introducing nitrogen into the metal boride comprises performing a plasma nitridation process to form the metal nitride in the PMOS region.

21. (original) The method of claim 18, wherein the metal nitride is one of M_XN_Y, $M_XSi_YN_Z$, $M_XAl_YN_Z$, and $M_WAl_XSi_YN_Z$, where M is one of Ti, Ta, Hf, Zr, and W.

22. (original) The method of claim 18, wherein the metal boride is one of M_XB_Y, $M_XSi_YB_Z$, $M_XAl_YB_Z$, and $M_WAl_XSi_YB_Z$ where M is one of Ti, Ta, Hf, Zr, and W.

23. (original) The method of claim 18, wherein the metal nitride is TiN and the metal boride is TiB_2.

24. (original) A method of fabricating PMOS and NMOS metal gate structures in a semiconductor device, the method comprising:

forming a gate dielectric on PMOS and NMOS regions above a semiconductor body;

forming a starting material above the gate dielectric in both the NMOS region and the PMOS region, the starting material being a metal nitride or a metal boride;

changing the starting material in a first one of the NMOS region and the PMOS region such that a metal nitride is provided above the gate dielectric in the NMOS region and a metal boride is provided above the gate dielectric in the PMOS region;

patterning the metal nitride to form an NMOS gate structure in the NMOS region; and

patterning the metal boride to form a PMOS gate structure in the PMOS region.

25. (original) The method of claim 24, wherein the starting material is a metal nitride, and wherein changing the starting material comprises introducing boron into the starting material in the PMOS region to change the starting material to a metal boride in the PMOS region.

26. (original) The method of claim 24, wherein the starting material is a metal boride, and wherein changing the starting material comprises introducing nitrogen into the starting material in the NMOS region to change the starting material to a metal nitride in the NMOS region.

27. (cancelled).

28. (currently amended) ~~The device of claim 27,~~ A semiconductor device comprising:

an NMOS transistor gate structure, the NMOS gate structure comprising a metal nitride structure and a gate dielectric between the metal nitride structure and a semiconductor body; and

a PMOS transistor gate structure, the PMOS gate structure comprising a metal boride structure and a gate dielectric between the metal boride structure and the semiconductor body, wherein the metal boride structure comprises a metal nitride material doped with boron.

29. (original) The device of claim 28, wherein the metal boride structure is one of M_XB_Y, $M_XSi_YB_Z$, $M_XAl_YB_Z$, and $M_WAl_XSi_YB_Z$ where M is one of Ti, Ta, Hf, Zr, and W.

30. (currently amended) ~~The device of claim 27,~~ A semiconductor device comprising:

an NMOS transistor gate structure, the NMOS gate structure comprising a metal nitride structure and a gate dielectric between the metal nitride structure and a semiconductor body; and

a PMOS transistor gate structure, the PMOS gate structure comprising a metal boride structure and a gate dielectric between the metal boride structure and the semiconductor body, wherein the metal nitride structure comprises a nitrided metal boride.

31. (original) The device of claim 30, wherein the metal nitride structure is one of M_XN_Y, $M_XSi_YN_Z$, $M_XAl_YN_Z$, and $M_WAl_XSi_YN_Z$, where M is one of Ti, Ta, Hf, Zr, and W.

32. (currently amended) The device of claim ~~27~~28, wherein the metal nitride structure comprises TiN and the metal boride structure comprises TiB_2.

33. (currently amended) The device of claim ~~27~~28, further comprising a conductive upper material above the metal nitride structure and above the metal boride structure.

34. (original) The device of claim 33, wherein the conductive upper material is poly-silicon.

35. (original) The device of claim 33, wherein the conductive upper material is tungsten.